Supplement to

Logic and Computer Design Fundamentals
4rd Edition[1]

TEXT ERRATA

Printing 1 - Version 4-2.1 (Updated 12/03/07)

Chapter 1

p. 33, Problem 1-17: Replace “1480” with “1460”

Chapter 2

p. 60, Figure 2-9 (b): Remove “1” from lower right square **(Added 11/28/2007)**

Chapter 3

p. 146, Problem 3-31: Replace “4” with “3” in “4-to-6-line decoder”

Chapter 4

p. 203, Problem 4-31: Replace “E” with “EN”
p. 203, Problem 4-36: Replace “4-33” with “4-21”
p. 203, Problem 4-37: Replace “4-34” with “4-33”

Chapter 5

p. 243, line 2: Change “*C*” to “*D*”, resulting in “$B(t + 1) = D_B = AX + DX = (A + D)X$” **(Added 11/28/2007)**
p. 248, Logic Diagrams column: Change “6-13” to “5-12” and “6-10” to “5-9” **(Added 11/28/2007)**
p. 251, Figure 5-28(a): Remove the arc on S_1 labeled 11/00 and change label on the arc from S_1 to S_2 from “10/11” to ““10/11, 11/00” **(Added 11/28/2007)**
p. 254, line 26 (output constraint 2): Change “T_{ij}” to “O_{ij}”**(Added 11/28/2007)**
p. 259, line 5 from bottom: Change “STOP” to “$\overline{\text{STOP}}$”. **(Added 11/28/2007)**
p. 292, Problem 5-46: Replace “5-11” with “5-10”

Chapter 6

p. 333, Problem 6-13: Replace “32 × 8” with “64 × 8”

Chapter 7

p. 382, Table 7-15, last line: Change “SP” to “SD” **(Added 12/03/2007)**
p. 386, step 6, paragraph 2, line 2: Replace “>” with “<”**(Added 12/03/2007)**
p. 386, step 6 paragraph 2, **the iterative logic circuit design is incorrect.** Instead of evaluating A > B, it finds the leftmost occurrence of A = 0, B = 1, ignoring the presence of a prior A = 1, B = 0. In fact, to do the A > B operation from left to right, requires two carries, e.g, one representing the leftmost occurrence of A = 1, B = 0, and the other representing the leftmost occurrence of A = 0, B = 1 provided the first carry is not 1.

Replace section 6, paragraph 2 beginning with “left to right” in line 3 with the following solution for an iterative circuit that uses a **single right-to-left carry**: “right to left, the equation for each cell is $C_i = A_i \overline{B}_i + (A_i + \overline{B}_i)\, C_{i-1}$. and the incoming carry $C_0 = 1$. This represents the carries in an unsigned binary 2’s complement subtractor using the circuit shown in Figure 4-7 with S = 1 to perform $A - B$. For this circuit, the result $A - B = A + (2^n - 1 - B) + 1 = 2^n + (A - B)$. If $A - B \geq 0$, then the result is $\geq 2^n$, and C_n (the carry out of the MSB) = 1. If A – B < 0, then the result is $< 2^n$, and $C_n = 0$. Thus, for A < B, $C_n = 0$, and ALTB= $\overline{C}_n$.” **(Added 12/03/2007)**
p. 404, Problem 7-11, line1: Change “7-13” to “7-14” **(Added 11/28/2007)**
p. 405, Problem 7-20, line 1: Replace “A” with “B”

Chapter 8

Chapter 9

p. 490. Problem 9-4: Delete “1” after problem number.
p. 496, Problem 9-25: Add “+” and “Hint: In order to address all eight registers, it is necessary to provide eight values of SB in the Instruction Register. Since the Instruction Register can only be loaded from memory, these “instructions” must be placed in memory temporarily during the instruction execution and loaded into the IR as data without using the usual instruction fetch.”

p. 496, Problem 9-26: Solution of this problem with the architecture available is too difficult and while it can be solved, any solution is highly impractical. The problem will be removed in the 2nd and subsequent printings of the 4th edition.

Chapter 10

p. 538, Problem 10-11: In Register indirect + increment, interchange R_i and R_j following LD. **(Reworded 11/28/2007)**

Chapter 11

p. 594, Problem 11-7: Change “1ABCDEF” to “01ABCDEF”
p. 595, Problem 11-20: Change “(c), (d), (a)” to “(a), (b), (c)”
p. 596, Problem 11-21: (a) Add: “Assume DR = SA.” (b) Add: “Assume SB = SA.”
(Page number changed 11/28/2007)

Chapter 12

Chapter 13

p. 660, Problem 13-4, Part (b): Delete final “F” from “48CF0FF”

Please e-mail errors to: crkime@writphotec.com. Thanks to those of you providing error information.